Defect Management

Unpatterned Wafer Inspection for Immersion Lithography Defectivity

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High-yield immersion lithography requires the ability to distinguish between patterning and stack-related defects, such as wafer and resist-coating/bottom anti-reflective coating (BARC) defects. Extensive optimization of an unpatterned inspection tool, combined with advanced defect source analysis software, enables clear observation of stack-related defects through careful partitioning of individual layer inspections.

The switch from dry to immersion lithography has important consequences regarding wafer defectivity. The immersion process introduces additional types of defects that are primarily related to the physical contact of the immersion fluid (water) with the wafer surface. This article refers to resist coating defects, as well as defects coming from the silicon wafer or the BARC, as “stack-related” defects, while other types are referred to as “immersion-specific” defects. Because the most common approach in the study of lithography-related defects is to make use of patterned wafer inspection tools, only patterning-related defects are revealed.

However, this does not allow distinguishing stack-related defects from immersion-specific defects. This article investigates wafer defectivity throughout the various process steps prior to and including lithography, in order to understand and characterize the origin and propagation of defects (size, class, location) through each of these process steps. This requires extensive metrology optimization.

Unpatterned wafer defect inspection was performed using various darkfield inspection tools including the Surfscan™ SP1™ and SP2, and a brightfield inspection tool (KLA-Tencor 2351™). Defectivity after patterning was evaluated on the same brightfield tool. The lithographic stacks were based on commercial 193nm resist with and without immersion-dedicated topcoats. Defect review and classification were performed by SEM and optical microscopy.

Lithography Stack Information

One of the most important concerns when switching from dry to wet lithography is to overcome the leaching of resist constituents into the immersion fluid, resulting in possible contamination of the lens. Previously, the introduction of a topcoat was the primary approach to making the dry resist applicable to immersion processing. Today, the introduction of a new generation of low leaching resists, such as the PAR-IM850 (Sumitomo) makes it possible to process without a topcoat. The reduced laser spot size of the SP2 along with its optimized collection angles and faster signal processing allows the system to achieve the necessary sensitivity at a production throughput suitable for monitoring these smaller defects in the litho substrate and films.
Defect Detection on Resist

Figure 1 shows the scattering intensity model of a 70nm polystyrene latex (PSL) sphere on a resist stack. A zero resist thickness, denoted on the graph, essentially represents the BARC layer on top of a bare silicon substrate. A 150nm resist thickness was used in the experiment. It is apparent that the SP2 provided a much higher scattering signal over all thicknesses than the SP1, illustrating better sensitivity of the SP2 for smaller defects. The SP2 was also better at detection of sub-100nm defects in the litho stacks.

Besides resist thickness, another parameter that affects the scattering signal for detection of defects is the choice of polarization of the incident and scattered light. The polarization configuration of P-U (P-polarized for the incident optics and Unpolarized for the collection optics) was selected for the specific resist stack thickness (150nm), as seen in figure 2. The figure represents the scattering signal of a 70nm latex sphere at a specific thickness. At any particular film thickness, the combined constructive and destructive interference effect requires selection of the appropriate optical configuration to achieve the best scattering signal for these thin resist stacks, ARC-29A and the PAR-IM850.

Having the choice of either normal or oblique incidence enables the detection of defects of specific types at different detection thresholds. Practically, the two incidence angles lead to different responses for a PAR-IM850 resist stacked on ARC-29A with silicon as substrate. Using Klarity Defect™, defect source analysis (DSA) can be used to compare defect locations on the two wafer maps to, in this case, a tolerance radius of 200µm (Figure 3). This map-to-map technique allows common and added/unique defects to be quantified on a histogram or identified on a wafer map. This technique was used throughout the paper to identify differences in capture rate between normal and oblique modes, and to show common and added/unique defects throughout the resist stack. In this case normal incidence appeared to give a higher number of additional defects. This is mainly due to a higher number of randomly distributed unique defects sensitive to the normal incidence inspection close to the detection limit. A second contribution came from the higher count of defects from clusters.

Figure 4 shows the comparison of the SP2 to the 2351 bright-field inspection results. The 2351 system’s 0.25µm pixel-size inspection of the resist (visible light, avoiding any exposure of the resist) gave a comparable sensitivity to the oblique illumination of the SP2. Again, a better result was observed using the normal illumination. The variation in defect counts was mainly due to the difference in cluster reporting.
Noise Suppression

The choice of polarization and collection angles is important for suppressing the noise contribution from surface roughness (source of N) induced by the wafer processing. Organic films typically contribute a high level of surface scattering at UV wavelengths, depending on the film-specific chemical composition. A built-in optical filter on the SP2 can suppress this surface scatter from photons carrying higher energy at the UV wavelength than ones at 488nm on SP1. Up to 50% of suppression of the background signal (haze) can be obtained.

The SP2 allows the selection of either 10% or 100% of the full laser power in the recipe to minimize any potential for material damage at UV wavelengths and high power dosage, for resists and other organic films. In order to compare the potential damage to the resist, and to try and understand the mechanism behind any changes, wafers with PAR-IM850 were scanned ten times using normal incidence with the optical filters off for 10% and 100% laser power. Figure 5 shows the average haze for the wide and narrow channels after each scan. 100% power was shown to change the haze by 7% and 5% for the wide and narrow channels respectively after 10 scans. The 10% level resulted in a minor change in the haze signal. The change in haze may be a surface modification due to solvent outgassing from the surface, a minor reflowing of the top surface or a chemical change in the resist. All inspections were for this reason performed at 10% laser power.

To check for modifications of the chemical bonding at 10% or 100% power, FTIR was used. The wafers, scanned with the SP2 (one scan and 10 repeated scans) were compared to a reference wafer that had not been scanned. No evidence was found for any SP2-induced change in photoresist composition or bond structure. These results indicated that probably some solvents were evaporating from the resist during the laser exposure.

Recipe Summary

Recipes for all resist stack layers in the study were optimized with the above considerations to achieve the best signal to noise. Table 1 summarizes the best available defect threshold (Latex Sphere Equivalent, LSE) with two sensitivity-determination methods. In all cases, the sensitivity achieved on the SP2 was better than that of the SP1, demonstrating the need for the use of SP2 for immersion lithography resist monitoring as design rules shrink. All scans on the SP2 were performed with the 10% laser power mode and the use of optical filters for both channels (wide and narrow).

<table>
<thead>
<tr>
<th>ARC-29A</th>
<th>S/N = 1.5</th>
<th>Capture rate &gt;95%</th>
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<tbody>
<tr>
<td>SP2 Wide Oblique</td>
<td>83nm</td>
<td>80nm</td>
</tr>
<tr>
<td>Narrow Oblique</td>
<td>94nm</td>
<td>84nm</td>
</tr>
<tr>
<td>SP1 Wide Oblique</td>
<td>95nm</td>
<td>64nm</td>
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<tr>
<td>Narrow Oblique</td>
<td>105nm</td>
<td>101nm</td>
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<table>
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<tr>
<th>PAR-IM850</th>
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<tr>
<td>SP2 Wide Oblique</td>
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<td>71nm</td>
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<td>Narrow Oblique</td>
<td>72nm</td>
<td>65nm</td>
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<tr>
<td>SP2 Wide Normal</td>
<td>76nm</td>
<td>69nm</td>
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<tr>
<td>Narrow Normal</td>
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<tr>
<td>SP1 Wide Oblique</td>
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<td>Narrow Oblique</td>
<td>82nm</td>
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<td>SP1 Wide Normal</td>
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</tr>
<tr>
<td>Narrow Normal</td>
<td>149nm</td>
<td>145nm</td>
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</table>

Table 1: Signal to noise versus capture rate for the different layers, comparing SP1 and SP2 versus normal and oblique for the ARC and resist. SP2 recipes were set at 10% laser power and optical filters for both channels.
Defect Analysis: Stack-Related vs. Immersion-Specific Defects

When monitoring an immersion lithography tool (ASML XT:1250Di) or process with particle per wafer pass (PWP) tests, a typical tool monitoring technique, it is important to be able to understand whether the defects are related to the resist stack or they are intrinsic to the immersion process itself. A clear distinction allows one to continue the ongoing improvement in defect reduction. Thus, a partitioning experiment was performed to allow the calculation of the impact of each layer on total defectivity and determine the impact of these defects on the overall pattern formation. An overview of the partitioning experiment is given in figure 6. Note that specific patterning defects were excluded from this study.

The starting material, bare silicon (MEMC – p Mon F130), was first inspected with a SP2 recipe at LSE >52nm including a crystal originated particle (COP) classification to determine incoming baseline defectivity. An ARC layer was coated on the silicon wafer, followed by a soft bake. This layer was inspected by the SP2 in the oblique mode for LSE >83nm. The following part of the stack consisted of a photoresist PAR-IM850 coating and soft bake. This layer was also inspected by the SP2 in normal mode at LSE >76nm. In some practical cases the intermediate inspection of the ARC layer was skipped. The next lithography processing step on the ASML 1250i was either a scan at zero exposure dose (simulating an immersion lithography process) or full exposure plus post-exposure bake and development to give the printed pattern.

Finally, defect maps before and after scan/development were compared, and a defect source analysis was performed on the results to distinguish between stack-contributed defects and immersion-specific defects.

In the experiment, the unpatterned wafer inspected area was 660.5cm², using high sensitivity mode, with 5mm edge exclusion. The patterned inspection used a different inspection area, determined by the number of available die on the wafer that could be inspected using the 2351 (556.18 cm²). This would have affected the results if defects had been found at the edge of the wafer; however, the SP2 inspection results showed that the majority of the defects were not from this region.

Scan at Zero Dose

After the stack formation, the wafer was scanned with water (in the ASML XT:1250Di) at zero dose to mimic a typical wafer passing under the immersion head, and determine the effect of the water flow over the wafer during exposure. The wafer was then re-measured on the SP2 to isolate immersion-related defects from the stack defects.

From the results in figure 7, the impact of each layer during the stack formation was observed. A map-to-map coordinate comparison at each step allowed the close examination of defects contributed from each specific process step with a significant number of defects were added during the immersion step.
A comparison stack tolerance set at 200µm (ARC and resist comprised one measurement). It was clear that a significant number of defects (>76nm LSE (optimized recipe)) were added during the immersion step. However, the various types of stack-related defects were not to be neglected. They were typically embedded in the resist. The final impact of these defects (stack-related or immersion-related defects) on the lithographic process is not known; a detailed study on the impact on patterning is required.

Exposed Wafer Tests (Regular Patterning), Example 1

To study the impact of stack-related defects on patterning defects, and distinguish them from immersion-related defects, the wafers were exposed and parallel lines were patterned in the resist. A parallel study was conducted using a wafer in which the stack was formed and measured in the same manner as above, except that the wafer was exposed with a small die (10x10mm$^2$) reticle, using exposure conditions to produce 100nm line/space features.

Defects originating from the incoming silicon wafer were traced through the ARC-29A coat step and the PAR-IM850 coat step, as illustrated in figure 8. The influence of the ARC-29A-defects was traced through the resist coat step and also the final develop and rinse steps. In this case ~30% of the defects inspected after pattern formation were attributed to the previous layer, with the resist layer having the highest influence. The remainder of the defects were attributed to current-layer patterning.

As indicated by the optical review results (Figure 9), the majority of the defects added during the resist coat step were particles in or on the surface of the resist. The
critical patterning defects (Figure 10) which later were found to originate at the resist steps were clearly mapped to a streak defect by the Surfscan SP2 SURFimage map — an enhanced haze capability on the Surfscan SP2 — earlier in the inspection steps. The defect cluster with its "comet tail" caused a high defect count.

More important, the small variation in resist uniformity can lead to a more significant effect of subsequent variation in line width due to a thinner-than-nominal resist layer, or a missing pattern in the worst-case scenario for patterned wafers. These defects were captured by a prototype algorithm outputting a defect feature vector of over 20 attributes (such as length, area, intensity, haze statistics, orientation, etc.) which was used for classification and defect binning.

The streak defect feature was extracted and displayed as figure 10b. This extraction of feature-only representation allows the defect to be exported for display in Klarity as a clustered, extended defect. The attributes are then available for Pareto’s, decision making, process control, etc. Figure 11 shows a different PAR-IM850 wafer with multiple streak defects, all of which were captured by the algorithm, although one streak was captured as two different defect segments. The length and area calculated by the algorithm for each defect are displayed in figure 11c.

**Exposed Wafer Tests (Regular Patterning), Example 2**

A second case, shown in figure 12, showed an improved defectivity level. In this case the influence of the stack-related defects was lower: ~5% of the defects originated from the substrate. Defects from the substrate appeared to be COPs.
detected during the brightfield inspection.

In this inspection the capture rate of the silicon defects in the ARC-29A was lower than that seen in the resist inspection or in the previous example. This was due to a slight change in the sensitivity in the ARC-29A recipe; however, the impact of the COPs/particles could be clearly seen during the resist inspection (Figure 13).

The defects seen as small, dark dots on the patterned inspection map were common to the defects seen during the SP2 silicon wafer initial inspection, mostly matching the spatial patterns of the COPs. The majority of defects observed on the BARC and resist were particles, as seen in figure 14.

**Conclusions**

For successful and efficient process control during immersion lithography, the capability to distinguish immersion/patterning-related defects from stack-related defects is very useful. The stack-related defects were observed only after careful partitioning of individual layer inspections and defect source analysis using Klarity.

The optimization of the unpatterned inspection tool, SP2, was central. Improved sensitivity at adequate signal-to-noise ratio was easily obtained on the resist stacks by using the shorter wavelength, UV-laser light of the SP2. For bare Si and BARC, oblique-incidence illumination gave better sensitivity and captured more defects. However, monitoring of the resist, and stacks with resist, required normal-incidence illumination for best scattering intensity.

The use of an optical filter and the 10% laser power setting also contributed to establishing a low, stable background signal for each inspection.

As immersion tool development is improved and immersion-specific defectivity is reduced, the proportion of stack-related defects will become a significant fraction of the overall defect count. A detailed method has been shown for the accurate monitoring of these stack-related defects. This includes point defects (embedded particles) or flow defects (streaks) identified and classified using SURFimage.

This information was used to identify the defect origin(s) for ultimate elimination of defects in the stacks. Stack defects continue to be important for either dry or wet lithography steps, as they have direct implications to the subsequent processing steps. However, determining the direct impact of individual stack defects on the final defectivity of the immersion process will require additional studies as the immersion process further improves and matures.