Enabling Manufacturing Productivity Improvement and Test Wafer Cost Reduction

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Use of a Surfscan SP2 inspection system can cut production costs by extending the reuse lifetimes of some monitor wafers and reducing the need for new test wafers. For a large foundry, this new technology can increase the in-house recycle rate and decrease the repolish rate by 15%, which translates to over $3M in annual savings.

Today's wafer fabrication plants must carefully balance the need to increase productivity while simultaneously reducing variable costs. There are a couple of main areas where process control (metrology and inspection) equipment can help minimize variable cost. The first is reducing consumables — minimizing the number of wafers that are processed for non-revenue operations, i.e., test wafers. Second is process equipment productivity improvements, by reducing the number of maintenance cycles per year and the associated time lost due to resolving process excursion false alarms. This article will explore these ideas in more detail, to determine an effective method for reducing test wafer cost in a leading-edge 65nm design rule foundry.

Process Tool Monitoring

Particle counts on unpatterned test (or 'monitor') wafers are typically used to monitor the health of process tools, either after preventive maintenance (tool qualification) or prior to running production wafers, after a specified number of hours or at the beginning of each shift (tool monitoring). Process tool qualification occurs after preventive maintenance or to requalify the tool after unscheduled downtime. Tool monitoring is used to quickly detect process tool excursions. Additionally, unpatterned wafer inspection tools can be used for engineering analysis work, either to characterize new process tools or diagnose specific contamination problems that led to a process tool being removed from production ('tool-down' problems).

Process tool monitoring uses a single unpatterned test wafer for each process chamber, with higher grade wafers used for front-end-of-line processes, where critical dimensions are smaller and greater inspection sensitivity is required. The test wafer is inspected, passes through the process tool (with or without activating the process chamber) and is re inspected. Added defects are calculated using a traditional post- minus pre-count calculation, or a more sophisticated map-to-map defect overlay comparison (reference 1). Post-scan inspection results reveal any defects added by the process tool, expressed as particles per wafer pass (PWP) added.

The Process Tool Monitoring Procedure

The first step of the process tool monitoring procedure is to assign the test wafers into bins by grade. Grade (usually A, B or C) refers to the quality of the test wafer appropriate for different monitoring applications, in this case its surface roughness, since smaller-size particles can be more reliably detected on smooth wafers than on rough wafers. Surface roughness is normally measured by using the inspection tool to detect haze, the low-frequency, low-amplitude component of the light scattered from the wafer surface. Haze is measured in ppm, a ratio of the average surface scattering intensity to the incident laser beam intensity. For bare wafers, haze is strongly correlated with surface roughness. (When a transparent film is present, haze also includes film parameter variation.)

The second step is the actual process tool monitoring step: comparing pre- and post-processing inspections and quantifying the added defects. In order to re-use the test waters, they are chemically stripped to remove any film layers and particles that were added by sending them through the process tools. The chemical stripping results in higher surface roughness or haze (the upper loop in Figure 1), and the test wafers must be regraded. After a certain number of recycle steps the test wafers fail the roughest grade specifications, and are then sent for reclaim (repolished) or scrapped (the lower left loop in Figure 1).
Extending the Useable Life of Monitor Wafers

Defect detection sensitivity is determined by the ratio of the defect signal to its background. As the background level (haze) approaches the detection threshold, the signal-to-noise ratio decreases (Figure 2, left). To ensure that defects can be detected without the occurrence of false alarms, it is desirable to keep a high defect signal-to-noise ratio, typically above 3.

However, as the number of chemical strips (recycles) increases the surface roughness and haze of the test wafer, the signal-to-noise ratio for detection of small defects on the wafer surface decreases. Manufacturing considerations such as matching one inspection tool's results to other tools dictate that the inspection sensitivity threshold remains at a fixed value. This means that the detection threshold cannot simply be increased to mitigate the increased background noise, as suggested in Figure 2 (right). Hence, the number of recycle steps that can be performed on any given test wafer is limited by this increase in surface roughness.

What is needed is a way to increase the inspection signal-to-noise ratio for small defects on rough wafers. The current generation wafer surface inspection system, the Surfscan SP2, has a smaller spot size than the previous-generation SP1, which means that less background is included when the spot is focused on a small defect. This gives the Surfscan SP2 better sensitivity on rough wafers than the SP1. Figure 3 shows a comparison of the same high-haze wafer, recycled many times, scanned using the Surfscan SP1 (left) and SP2 (right) systems. The SP1
map shows a significant population of false defects caused by the low signal-to-noise value. The inspection threshold, set to capture the real defects, is also capturing the peaks of the haze signal. On the other hand, the SP2 map shows significantly fewer false defects, since its superior sensitivity allows the scan threshold to be set well above the haze level. The capability of the Surfscan SP2 to enhance signal and better suppress noise enables this type of inspection, in turn allowing test wafers to be recycled for a longer period of time before they are reclaimed or scrapped.

Figure 4 shows signal-to-noise analyses for SP1 and SP2 on wafers of varying haze levels. The acceptable “inspection window” is at the upper left portion of the chart (better than 88nm sensitivity at S/N ratio ≥ 3). The SP1 high throughput mode cannot meet the 3:1 signal-to-noise requirement at the required 88nm defect sensitivity on high-haze wafers. SP2’s enhanced sensitivity and background noise suppression is able to meet the required sensitivity, even when using high-haze wafers, in high-throughput mode.

**Economic impact**

Figure 4 shows that the Surfscan SP2 can achieve sufficient sensitivity and signal-to-noise on rougher wafers; as a result, a dedicated SP2 inspector was placed into the in-house reclaim center in the fab where these measurements were taken. Wafers that would have been in the Grade B category for Surfscan SP1 inspection are now in the Grade A category for SP2 inspection. Consequently, wafers can be recycled more times – the recycle rate in the in-house chemical clean center was estimated to have increased by 15%. This higher recycle rate corresponds to a decreased reclaim (repolish) rate (Figure 5).

Using these new recycle rates, we can estimate the cost savings as follows, for a 300mm foundry running 25K WSPM, with test wafer usage equal to 3x the production rate, or 75K WSPM. Surfscan SP2 implementation increases the in-house recycle rate and decreases the reclaim rate by 15%, which translates to approximately $3M in annual savings for this case (Table 1). The model can be adjusted to accommodate different wafer starts, test wafer usage, etc.

**Summary**

Wafer fab productivity benefits from reduction of variable costs. Test wafer lifetimes directly impact their usability for process tool monitoring. Using a Surfscan SP2 inspection system instead of a previous-generation tool has been shown to enable further reuse of some monitor wafers, which also reduces new test wafer purchases. In addition to the quantifiable economic impact of test wafer cost reductions, fab manufacturing productivity also increases, while disruptions due to false excursion alarms resulting from unstable inspection results of roughened reclaimed wafers are minimized.

**Acknowledgements**

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Table 1: Estimated monthly cost savings from increased wafer recycle rate: $0.28M, for an annual savings rate of $3.36M.

**References**

1. Lorrie Houston, Motorola; John Anderson, Motorola; Rhonda Stanley, KLA-Tencor; “Process tool qualification using SP1TBI automated overlay feature,” KLA-Tencor Surfscan Applications Note (2002).