Toward Zero Defect: Automotive Fab Best Practices for Assessing "Best Performing Tools"

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Agenda

1. Introduction
2. Process Tool Capability
3. Process Tool Defectivity
4. Summary and Recommendations

KLA: Quality Partner for the ICs that Power the Future of Automotive

Automotive Commitment and Expertise

Ann Arbor, MI

- R&D Center
- Automotive and AI

Commentary

- Process Watch
- Semiconductor Engineering
- ECN, Elektronik, …

Workshops

- Auto fabs
- Tier 1s
- OEMS

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Quality Control Solutions for Automotive ICs

Continuous Improvement

- Surfscan® Series

Zero Defect Screening

- 8 Series
- Certified and Relaunched

Advanced Design Node

- 39xx and 29xx Series
- eDR7xxx™ Series

Packaged IC Quality

- ICOS™ Series

Power Device Reliability

- Candela® CS920

The Appeal of a "Best Performing Tool" Program

Imagine a fab with two tools at every process step

Tool A has 99.99% yield at each step

Tool B has 99.7% yield at each step

		Process Step Number																											
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	185	186	187	188	189	190	191	192	193	194	195	196	197	198	199	200
Tool A	99.99%	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Tool B	99.70%	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B

Can choose between A or B at all 200 steps

Impact on Final Yield

Best Performing Tool Path
Random Path

Final Yield

		Process Step Number																														Final Yield
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	185	186	187	188	189	190	191	192	193	194	195	196	197	198	199	200	
Tool A	99.99%	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	73.3%
Tool B	99.70%	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	

		Process Step Number																														Final Yield
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	
Tool A	99.99%	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	74.4%
Tool B	99.70%	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	

		Process Step Number																														Final Yield
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	
Tool A	99.99%	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	75.5%
Tool B	99.70%	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	

		Process Step Number																														Final Yield
		1	2	3	4	5	6	7	8	9	10	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	
Tool A	99.99%	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	84.8%
Tool B	99.70%	B	B	B	B	B	B	B	B	B	B		B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	

This is the "Best Performing Tool" Effect

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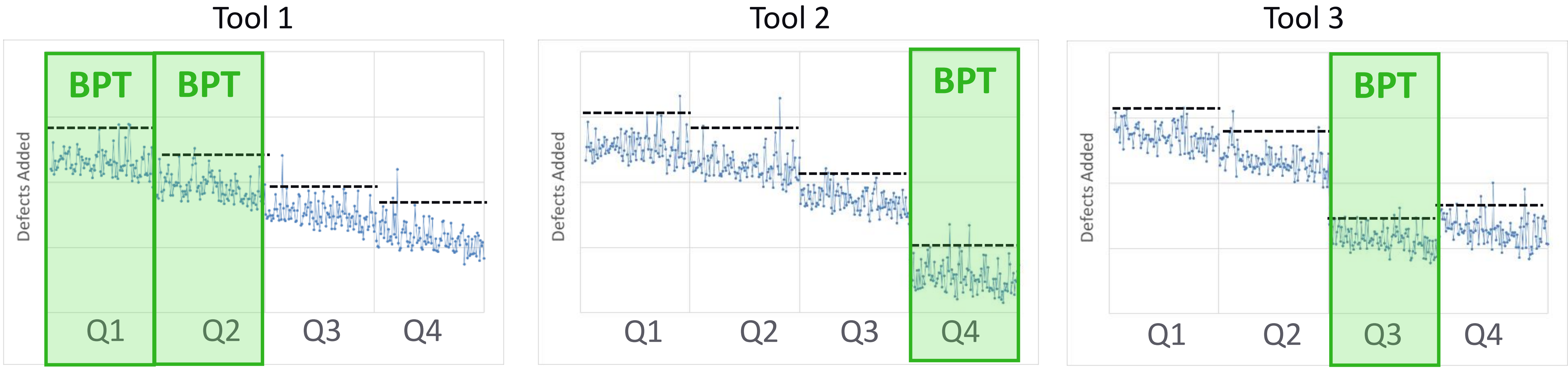
Always Start with a Fab-wide Yield Improvement Program

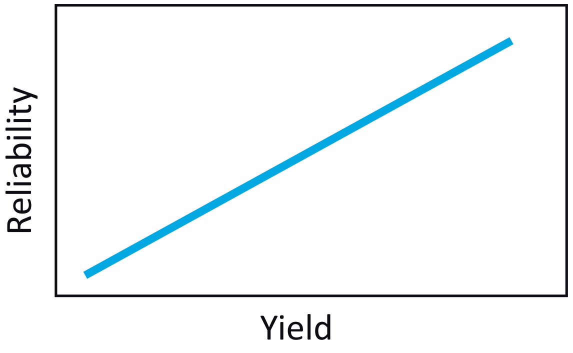


- Fab wide yield improvement is a long process (measured in quarters)
- The Best Tool frequently changes as the fab improves
- The goal is find the best tool wherever you are on that journey

The data needed to identify Best Performing Tools (BPT) flows naturally out of a comprehensive continuous improvement program

What is the Criteria for "Best Performing Tool"

1. Tools with High Step-Yield
   - Tool commonality analysis: de-convolve final wafer yield to the tool level
   - Time lag: tells you how the tool performed 1-3 months ago

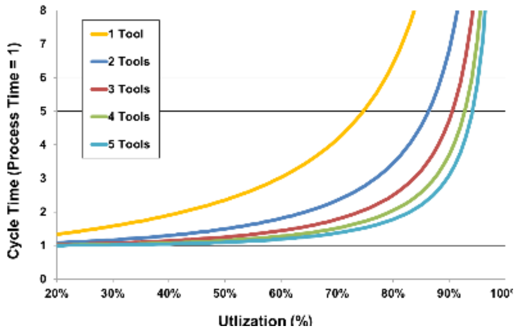


2. Tools that are Available
   - Cycle time and queue time can be driving factors if there is only a single tool that is allowed for a given step.
   - Best tool → Best available tool

3. Process Tool Capability
   - Process window >> total variability
   - Measurement system capability

Focus of this Paper

4. Process Tool Defectivity
   - Fewer added defects (all types)
   - Sufficient inspection sensitivity and sampling



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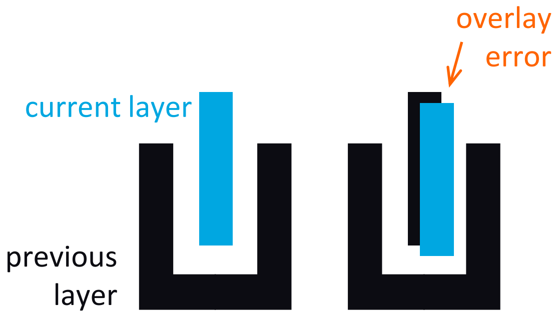
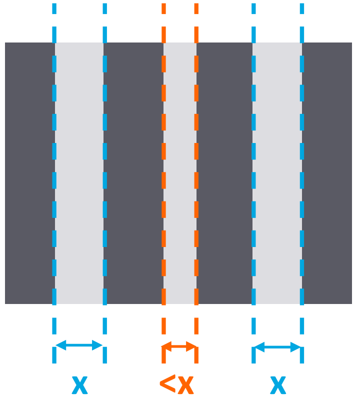
Common Process Control Measurements

On Product Overlay

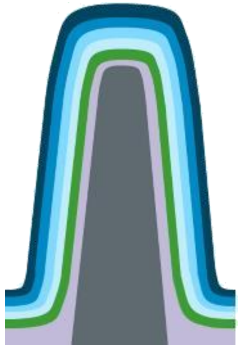


top down view

Critical Dimension Uniformity



Film Uniformity



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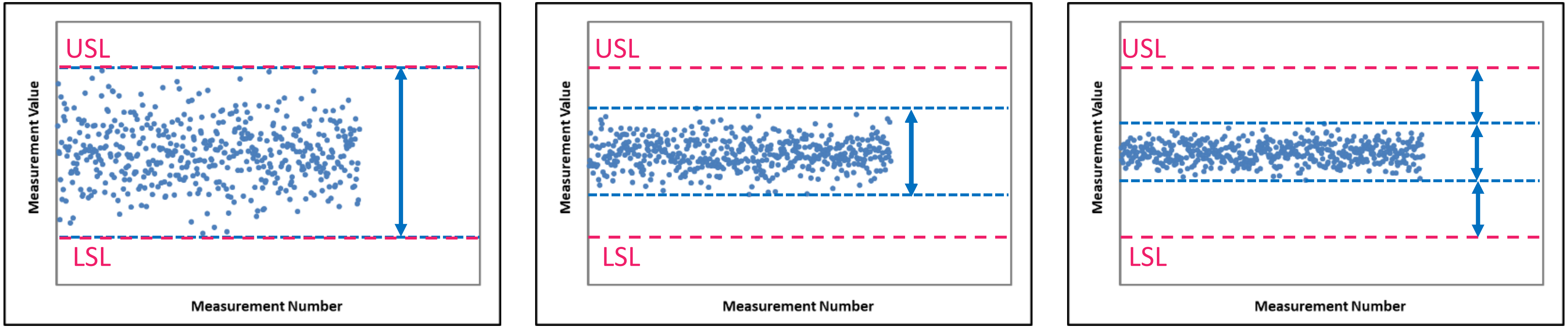
Understanding C_p (Process Capability Index)



$C_p = 1.0$ $C_p = 2.0$ $C_p = 3.0$

C_p is a measure of how well the natural process variation fits within the spec limits

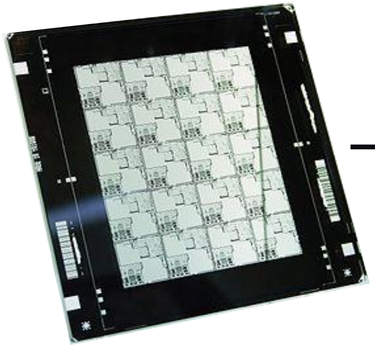
$$C_p = \frac{(USL - LSL)}{6\sigma}$$

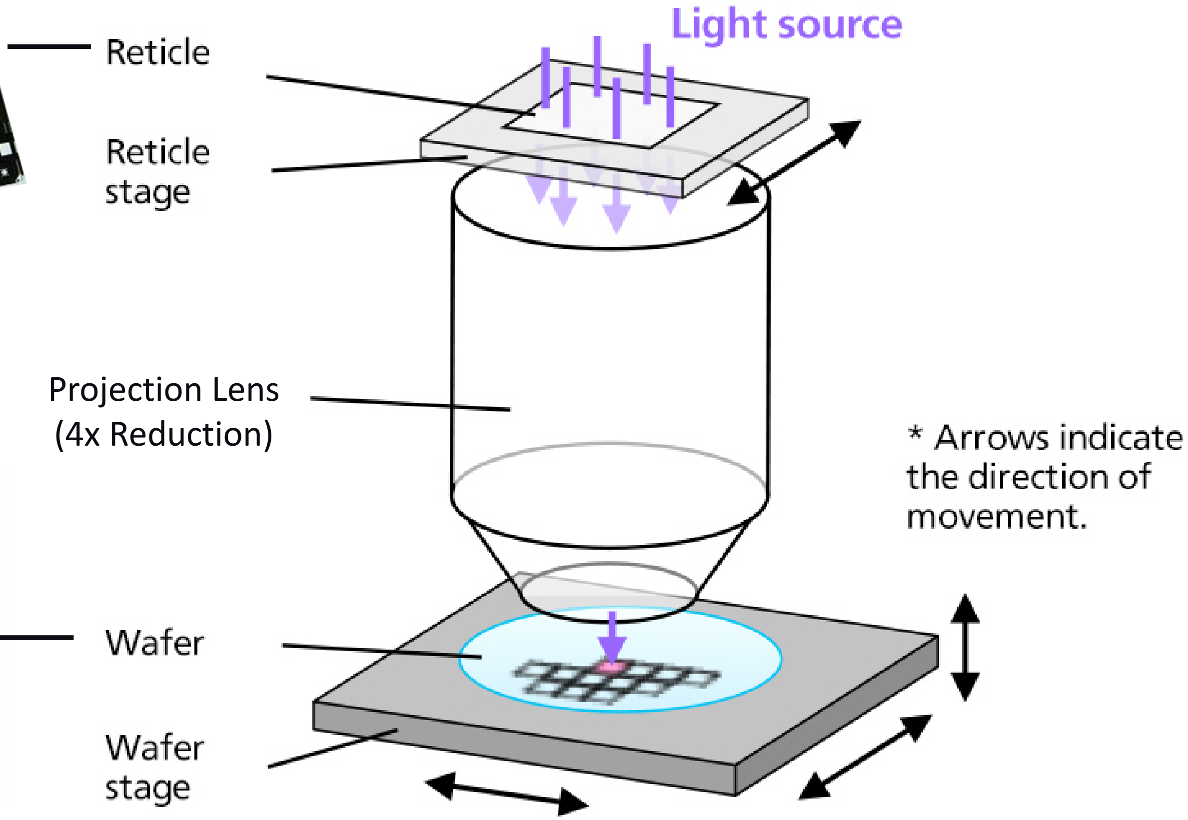
USL = Upper Spec Limit
LSL = Lower Spec Limit
σ = Standard Deviation of the Process

Challenge of Assessing C_p for a Process Tool: Litho Example

Reticle (Mask):

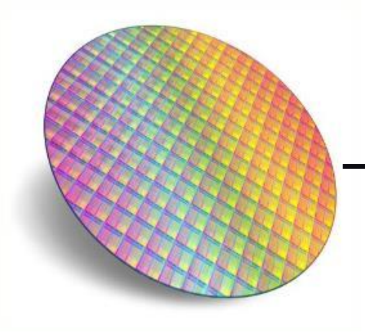
- 1 field
- 1-100 die (or more)
- 10 Billion transistors





Wafer

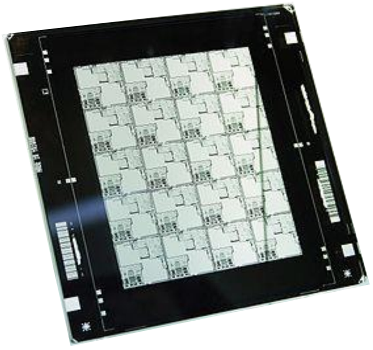
- 100 fields
- 1000 die (or more)
- Trillion transistors



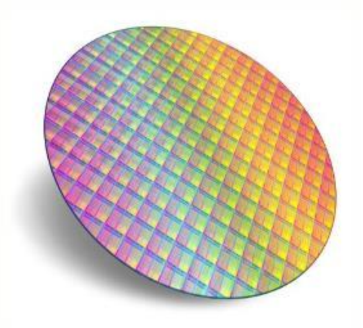
Most fabs measure 5 to 50 locations

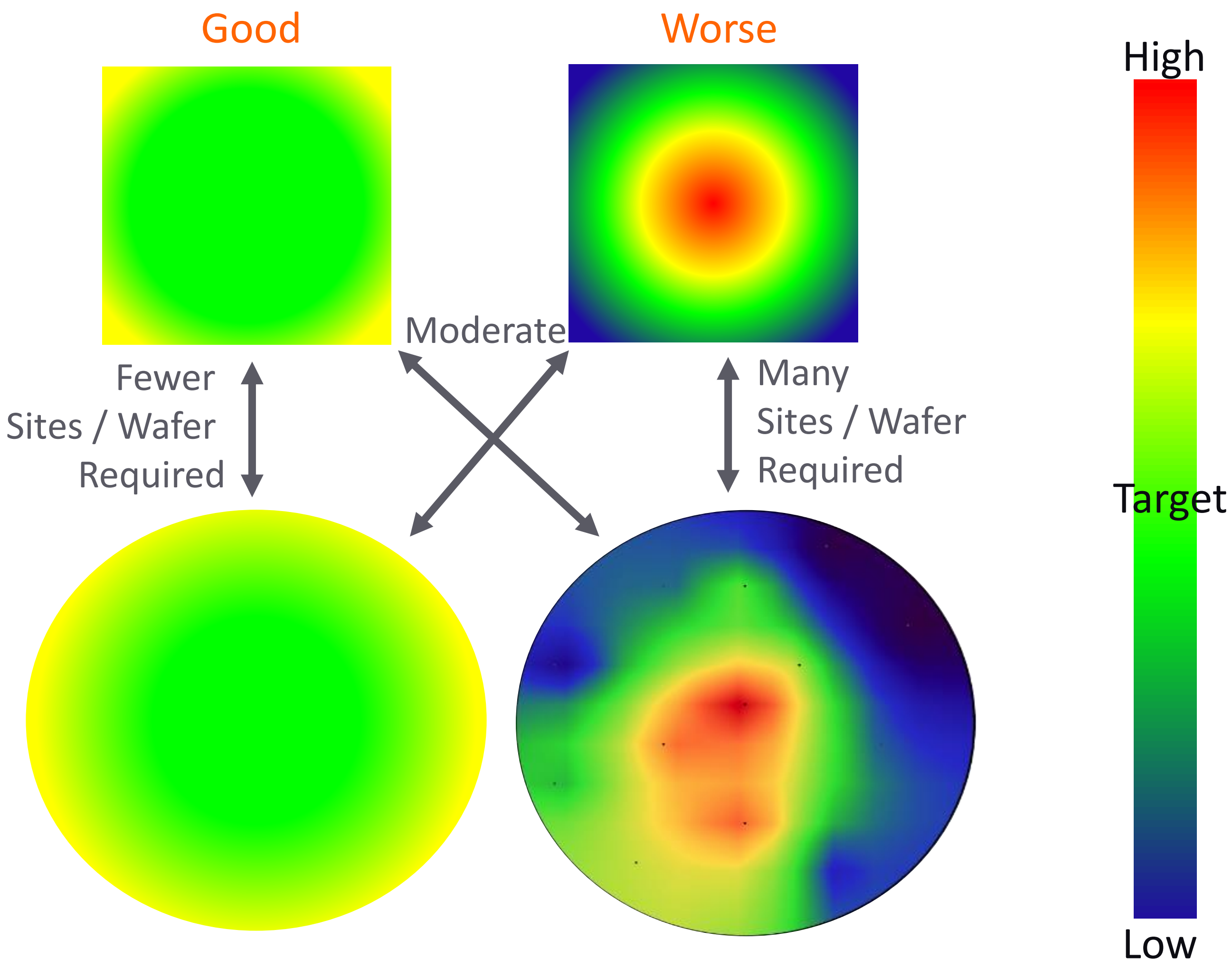
Complex Sources of Variability

ACLV: Field
Across ~~Chip~~ Line Variation



Cross Wafer Line Variation

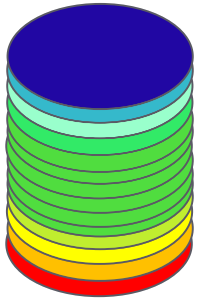




Site Sampling Plan Must Reflect The Combined Variability

Sources of Variability II

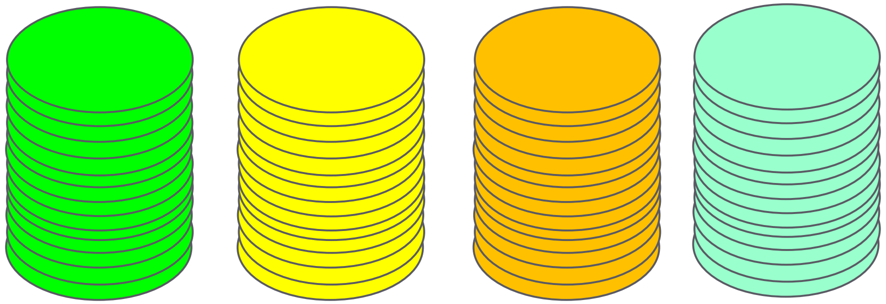
Wafer-to-Wafer Variability



Wafer-to-wafer Variability within a lot

- First wafer effect
- Last wafer effect
- Every nth wafer
- Rogue wafer
- Random
- Tool Maintenance

Lot-to-Lot Variability



Lot-to-Lot Variability within the line

- Fab temperature
- Humidity
- Vibration
- Rogue Lot
- Random
- Tool maintenance

Wafer and Lot Sampling Plan Must Reflect The Combined Variability

Finding the Best Performing Tool: C_p

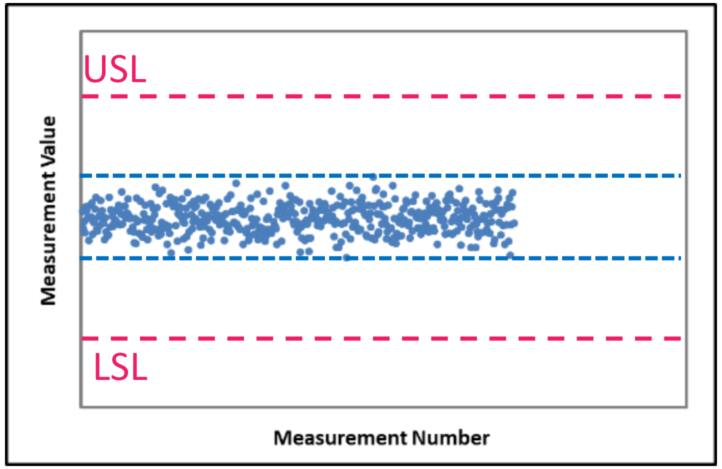
Field

Across ~~Chip~~ Line Variation
Cross Wafer Line Variation
Wafer-to-Wafer Variation
Lot-to-Lot Variation
Measurement-Tool Precision
Sampling Plan

C_p

(Sites per Field, Fields per Wafer, Wafers per Lot, % of Lots)

Is this the best performing tool?



- The sampling plan must capture the sum of all sources of variation
- The sampling plan must calculate the correct average for the lot
- The more variable a component is, the more measurements should done at that level

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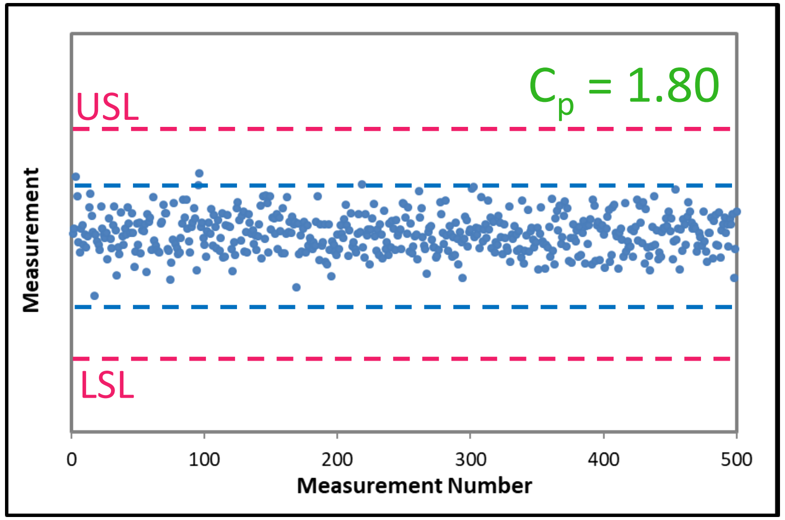
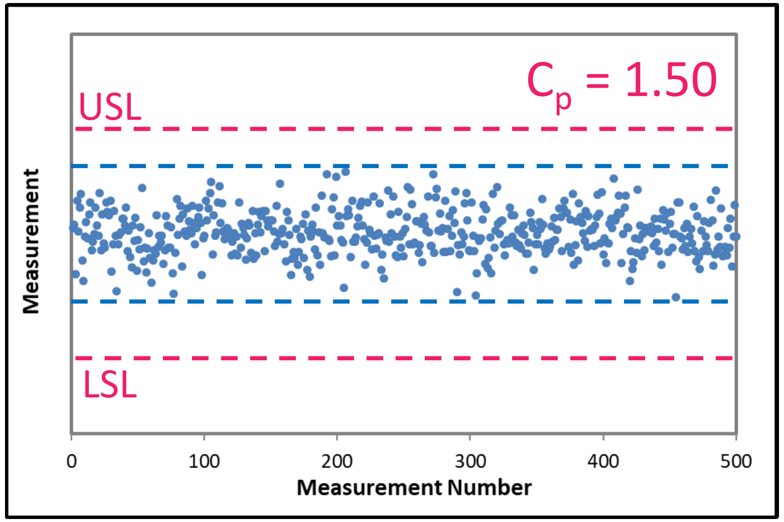
Tool With Best C_p

Tool A



Tool B



18 Sites / Wafer; 5 Wafers / Lot

13 Sites / Wafer; 2 Wafers / Lot

With this sample plan, Tool B has higher C_p

Both are worse than thought, but Tool A has higher C_p

Summary Table

	Sources of Variation in The Measurement					Applicable Tool Set			
Measurement	**ACLV (X-Field)**	**X-Wafer**	**Waf-2-Waf**	**Lot-2-Lot**	**Sample Plan**	**Litho**	**Etch**	**Films**	**CMP**
Critical Dimension	**X**	**X**	**X**	**X**	**X**	**X**	**X**		
Film Thickness		**X**	**X**	**X**	**X**			**X**	**X**
Overlay	**X**	**X**	**X**	**X**	**X**	**X**			

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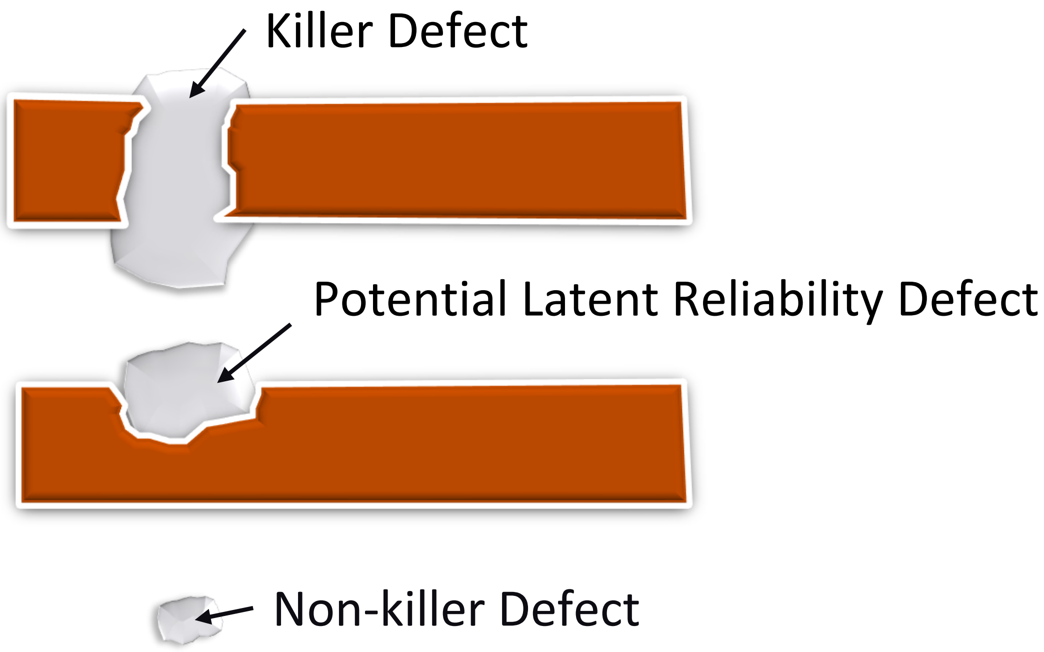
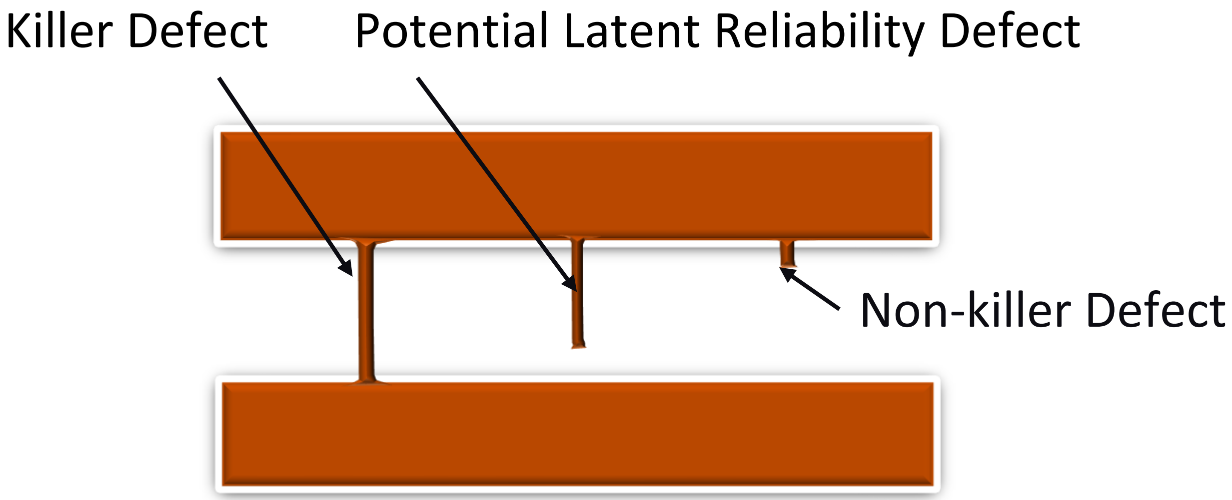
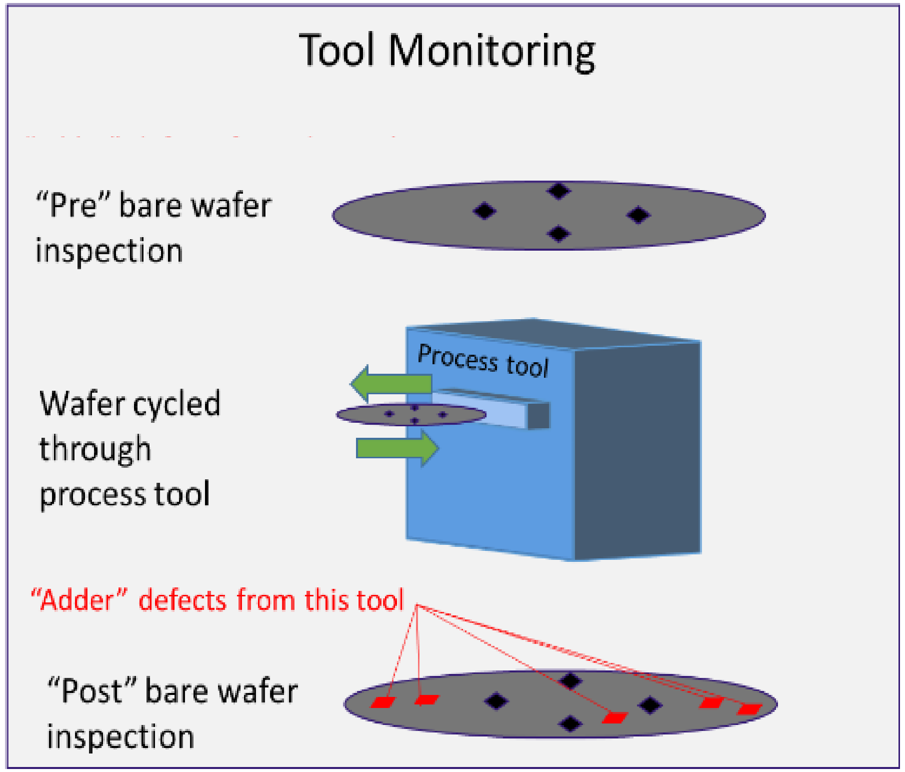
Automotive Reliability Defects

1. Killer defects in test coverage gaps
2. Latent reliability defects which become activated after test

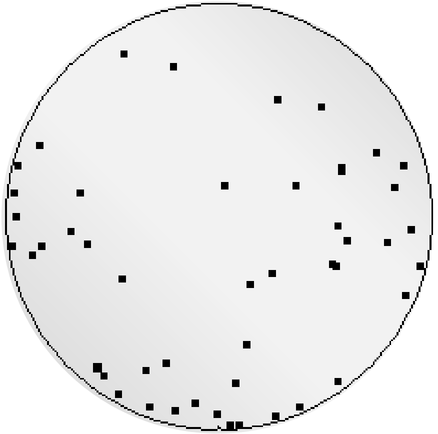




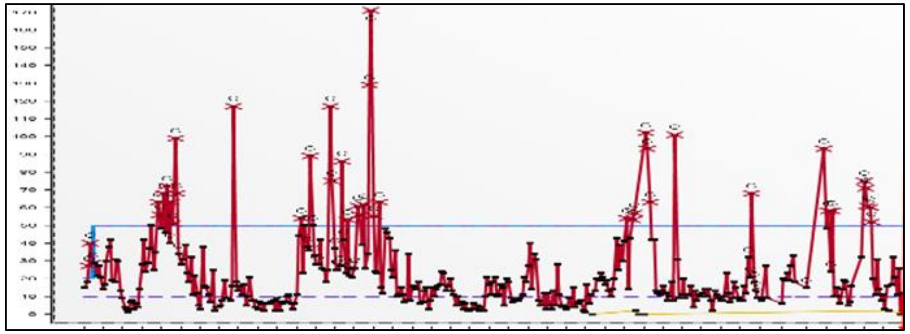
Quantifying Defectivity



- Most mature process defectivity comes from random defects from process tools
- Monitored using blank test wafers or using production material
  - Pre / Post inspection and subtraction
  - Mechanical and process step contribution



Defect Wafer Map

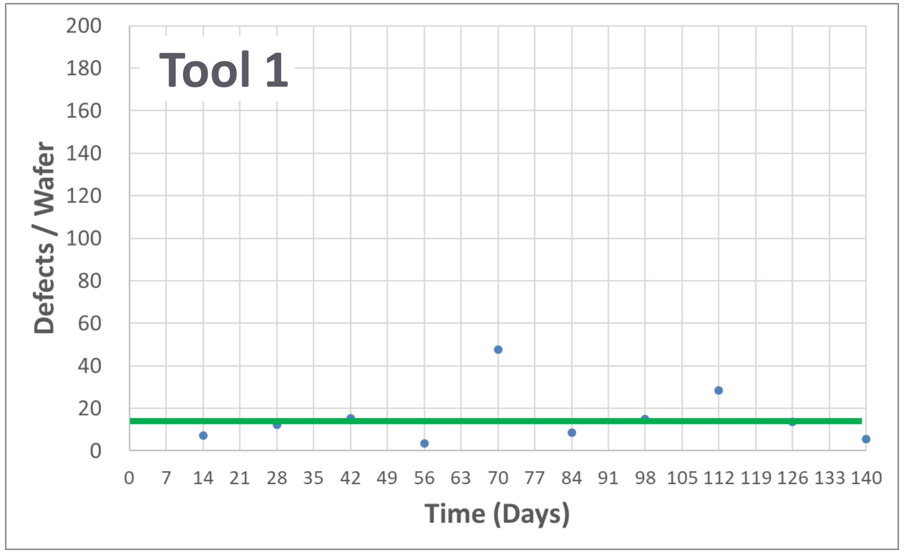


Tool Defectivity SPC Chart

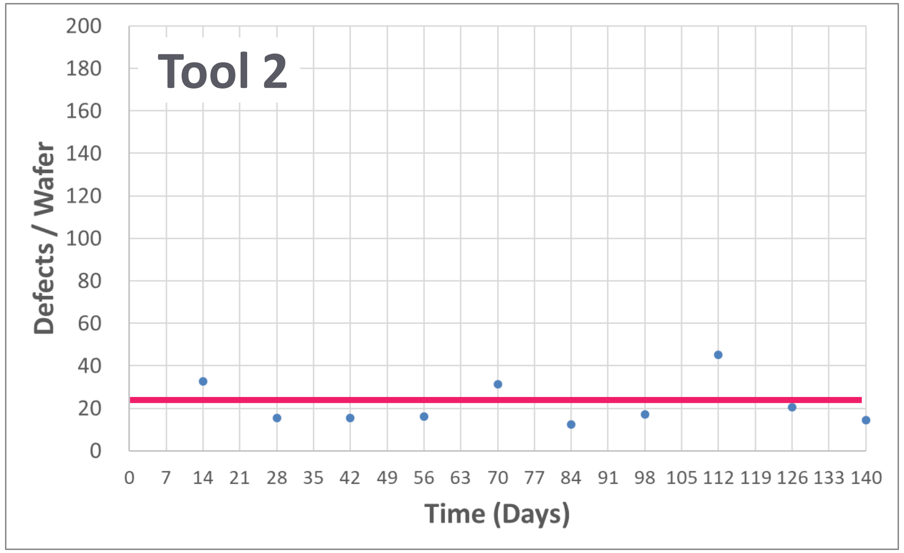
Finding the Best Performing Tool: Defectivity

Is There Enough Data?

Qual Frequency: **Every Other Week**



Mean = 16



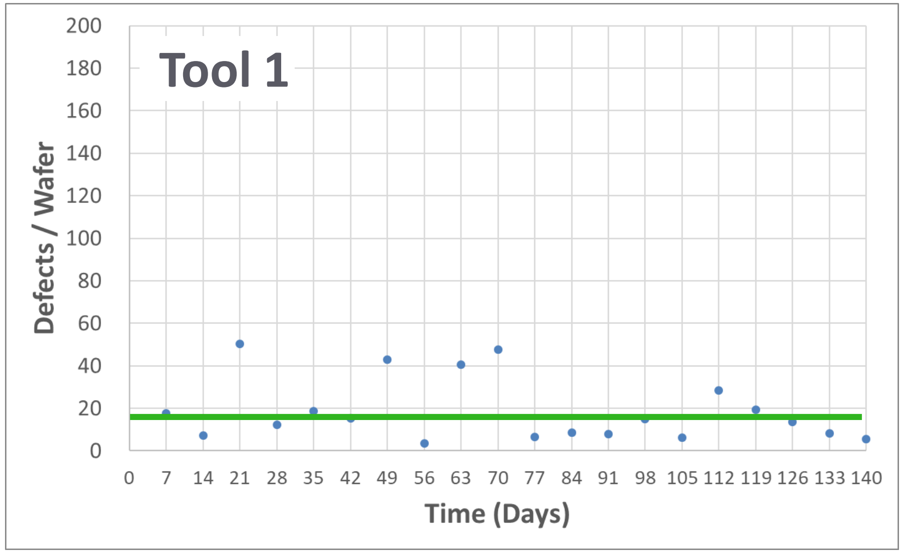
Mean = 22

With sparse data Tool 1 appears to be cleaner

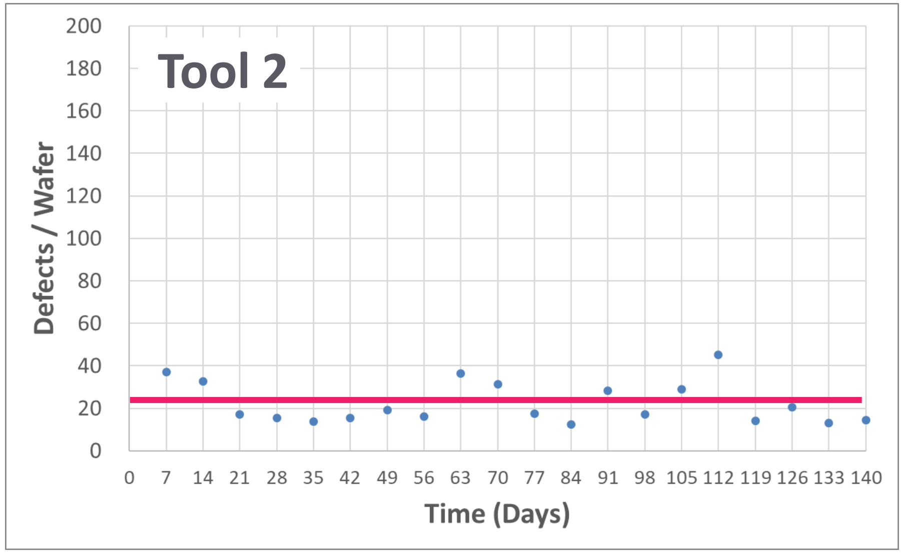
Finding the Best Performing Tool: Defectivity

Is There Enough Data?

Qual Frequency: **Every Week**



Mean = 18



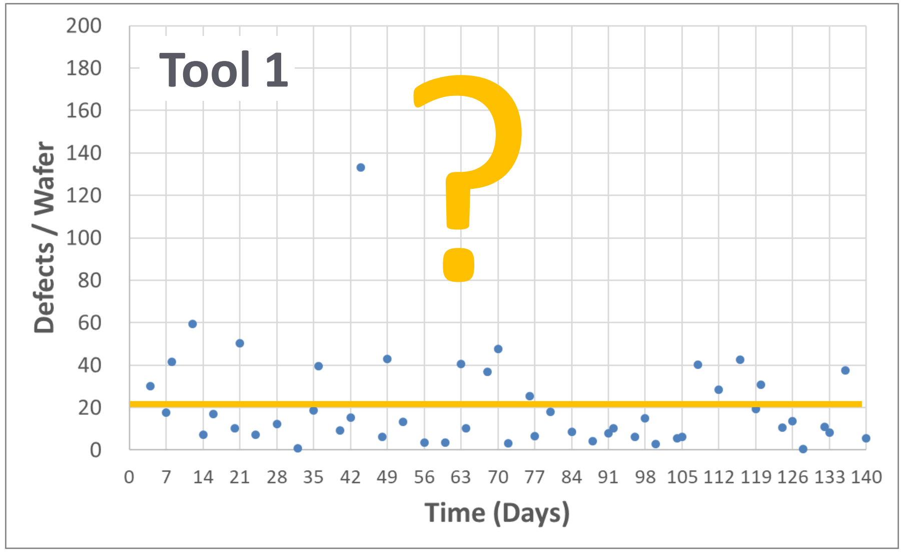
Mean = 22

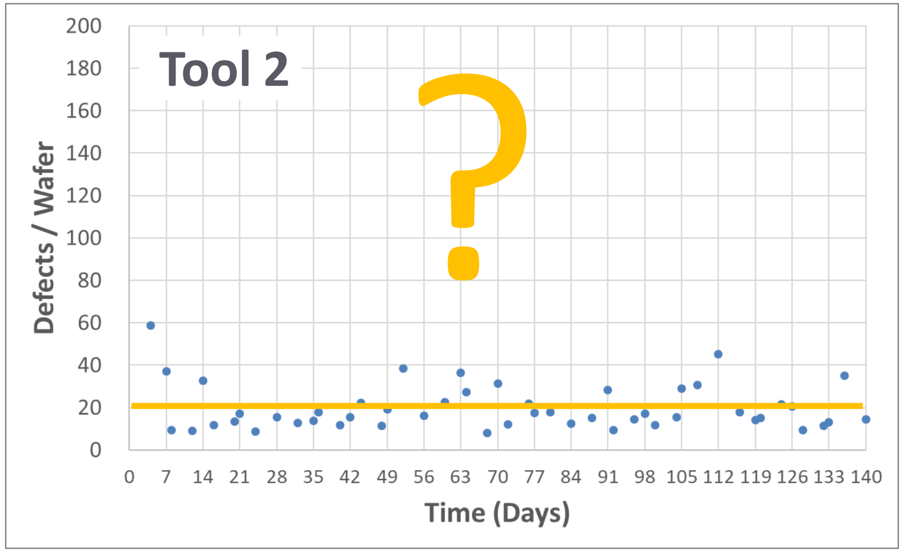
More variability but Tool 1 is still cleaner

Finding the Best Performing Tool: Defectivity

Is There Enough Data?

Qual Frequency: **Every 4 Days**





Mean = 21

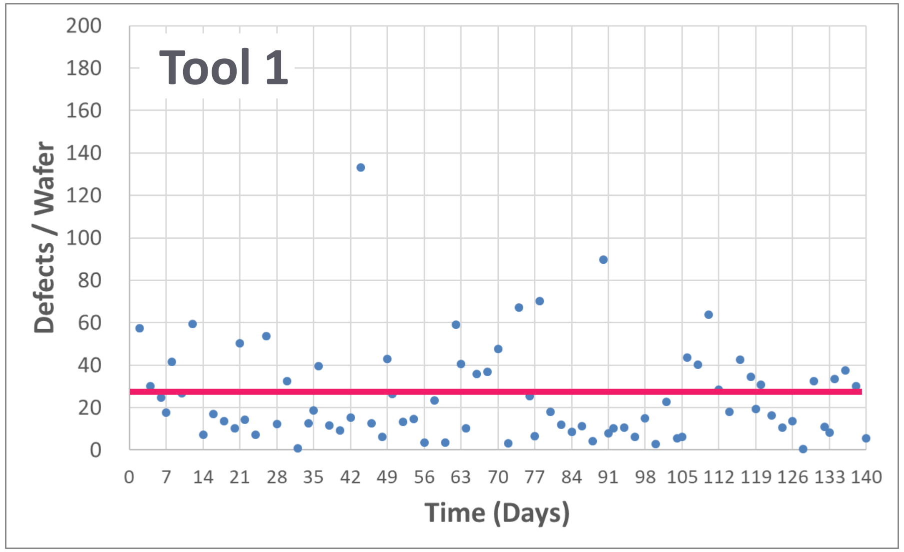
Mean = 20

Hard to tell the difference

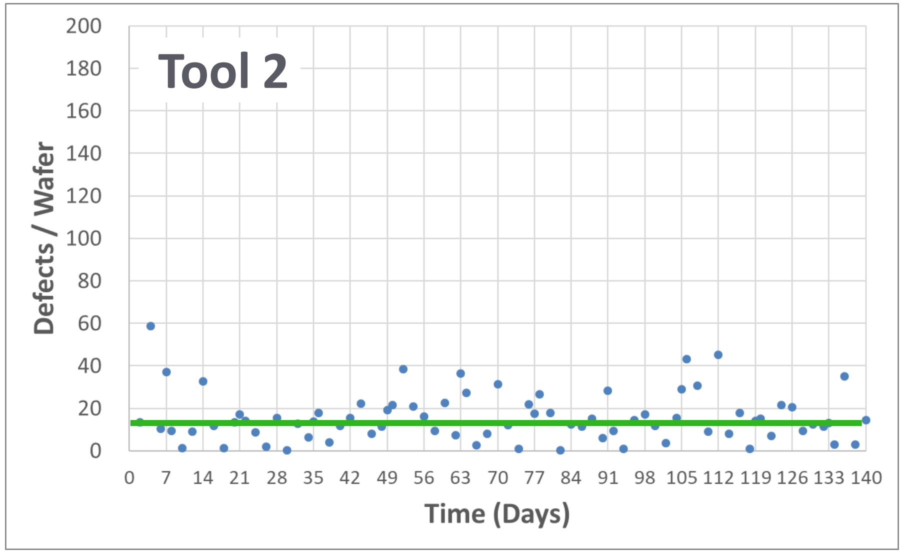
Finding the Best Performing Tool: Defectivity

Is There Enough Data?

Qual Frequency: **Every 2 Days**



Mean = 25



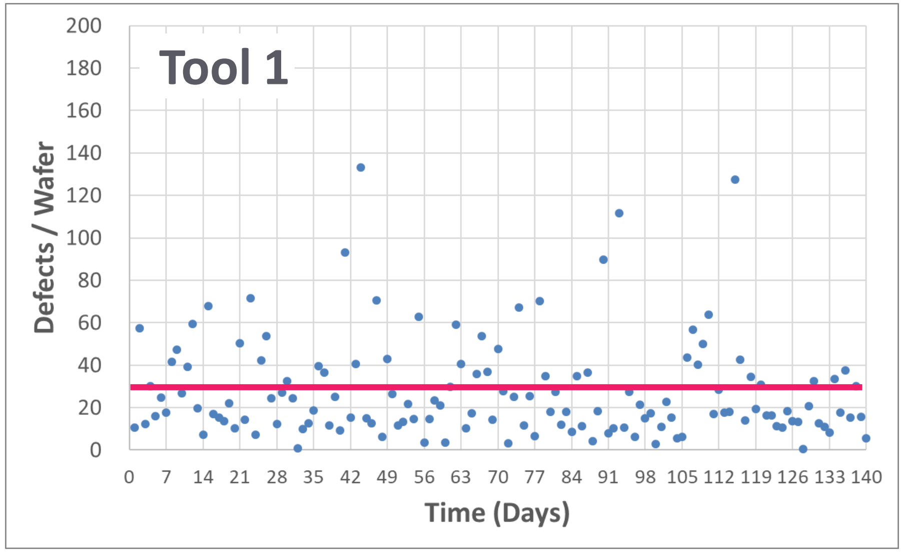
Mean = 15

More data highlights the variability in Tool 1

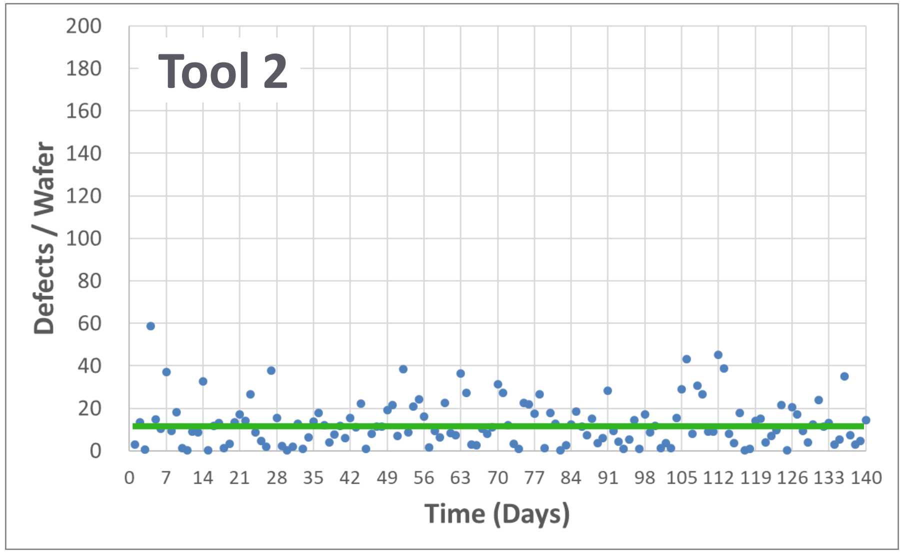
Assessing the Best Performing Tool: Defectivity

Is There Enough Data?

Qual Frequency: **Every Day**



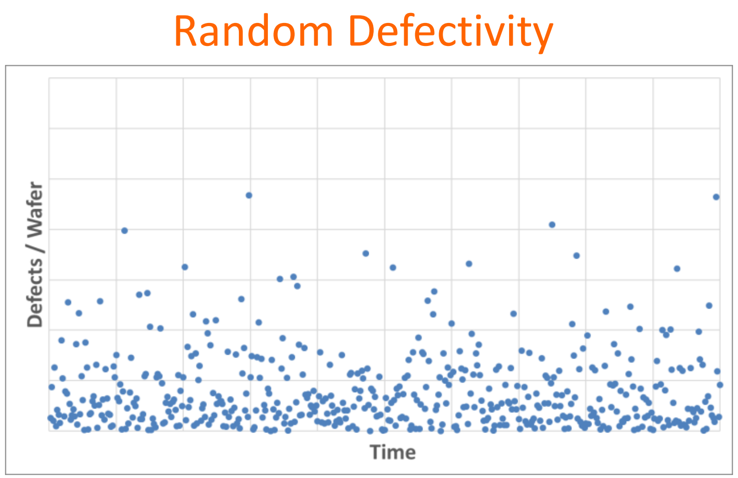
Mean = 28

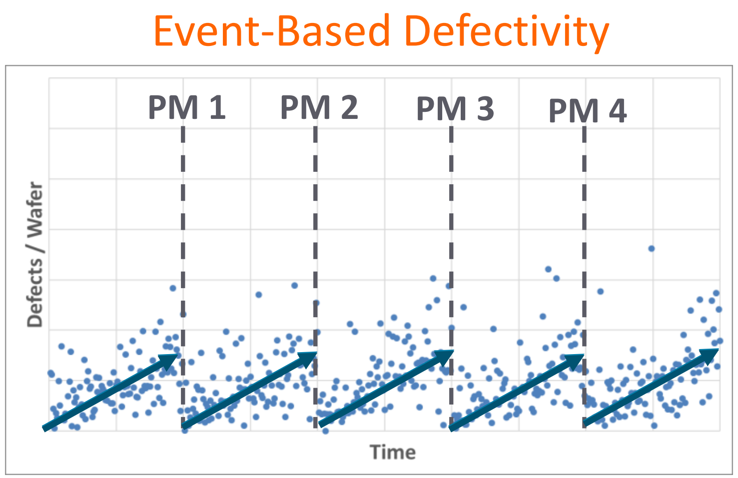


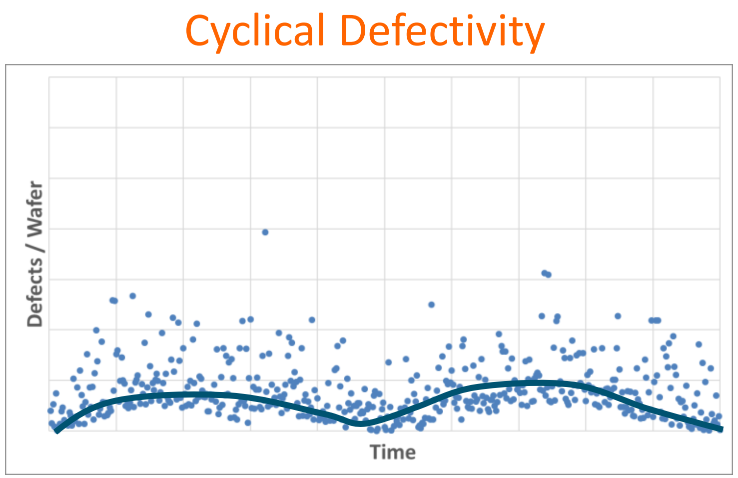
Mean = 13

Must collect enough data to capture potential patterns

Time-Based Defect Patterns



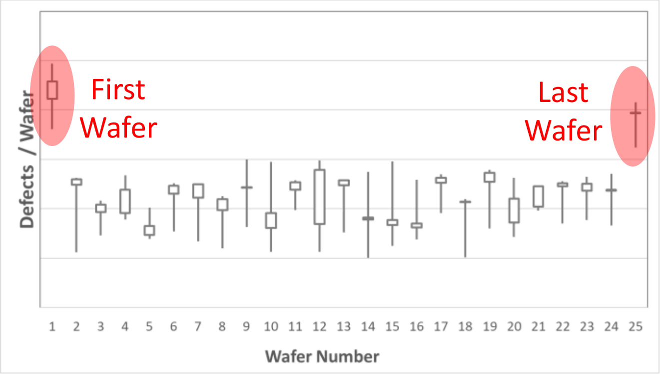




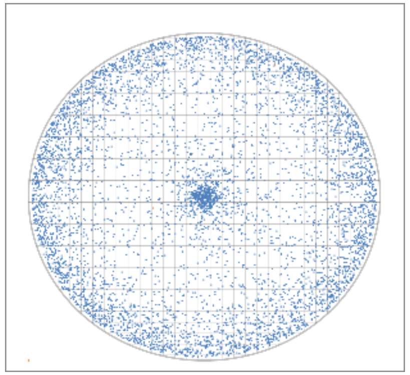
There must be enough data to identify these patterns (or rule them out)

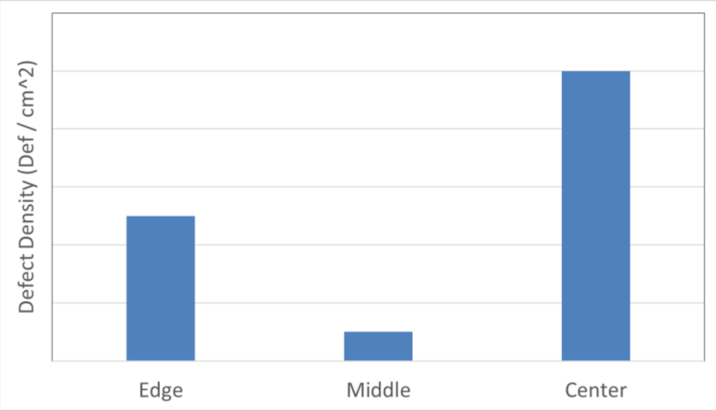
Position-Based Defect Patterns

Within-Lot Patterns



Within-Wafer Patterns

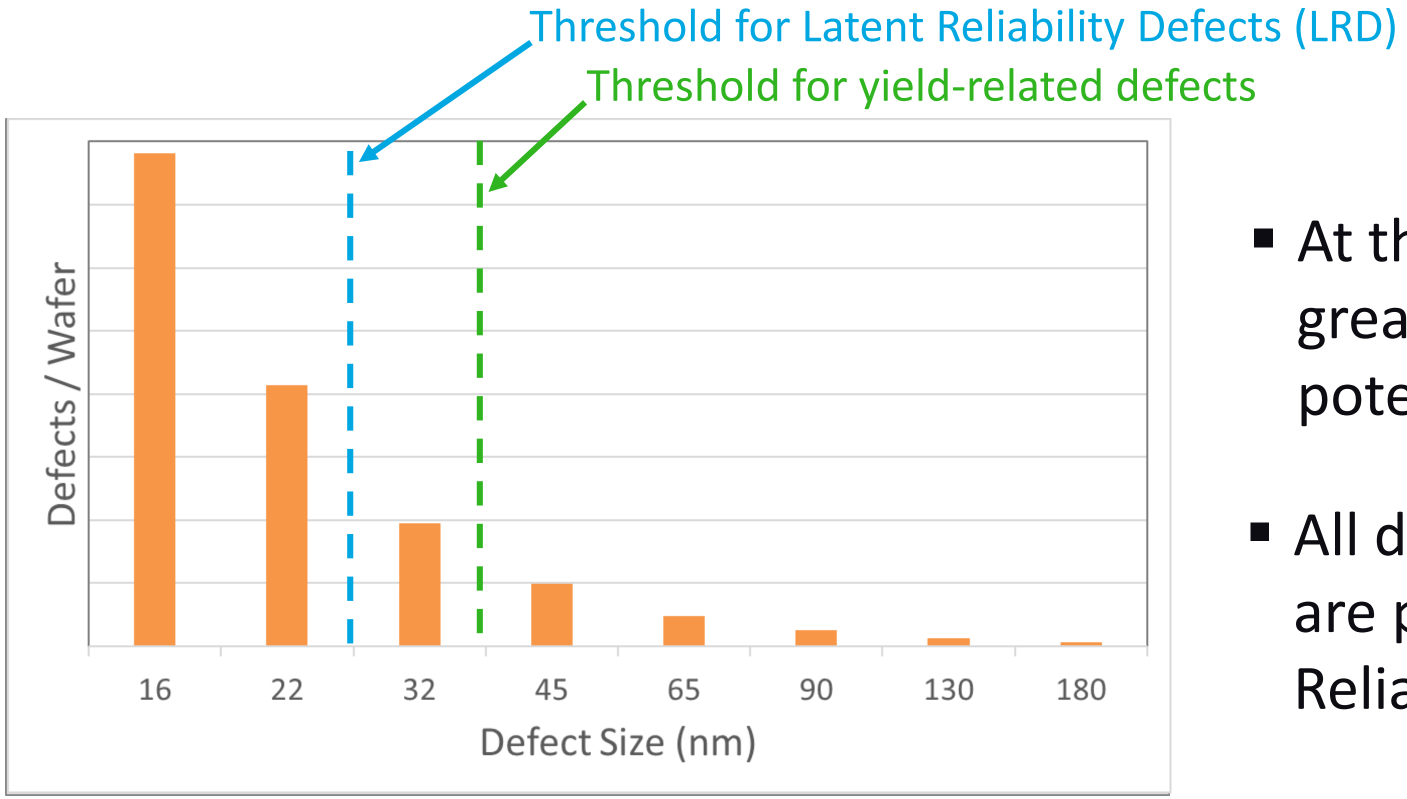




The defect density is as important as the defect count

- Is it concentrated in select wafers?
- Is it concentrated in select regions of the wafer?

Stapper Equation



Defect count is proportional to $1/X^n$ where X is the defect size

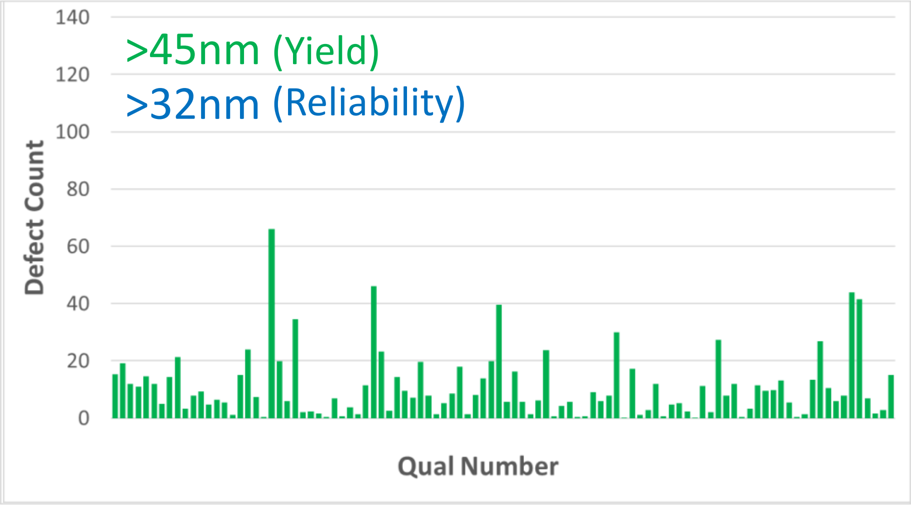
- At the 45nm DR, all defects greater than 45nm are potential killers
- All defects greater than 32nm are potential Latent Reliability Defects (LRD)

LRD's are typically a full design rule smaller than yield killers

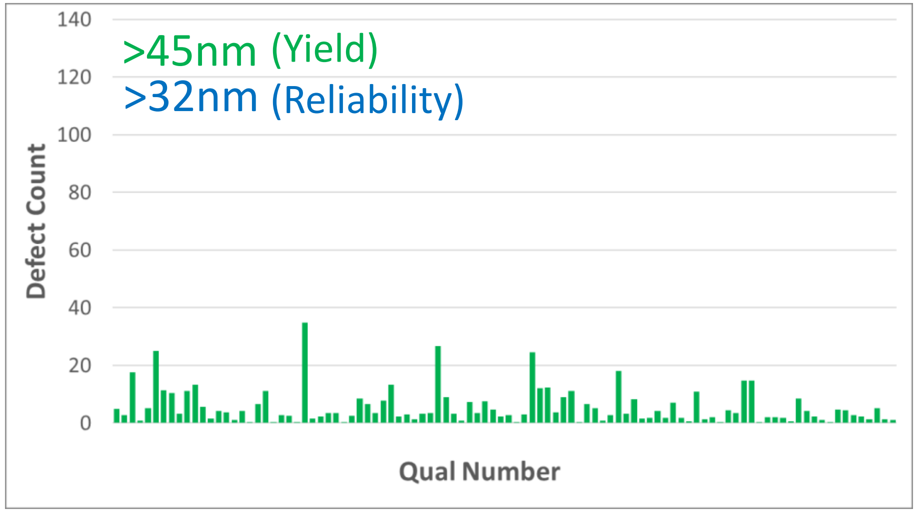
Sensitivity

Daily Process Tool Qual Results

Tool # 1



Tool # 2



Which tool is cleaner? It depends on the inspection sensitivity!

You need to monitor both thresholds: Yield & Reliability

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Summary

1. The best way to reduce reliability escapes is a fab-wide commitment to reduction in defectivity and process variability. A Best Performing Tool program can be layered on top of this to find the optimum tool at that particular point in time.

2. The Best Performing Tool is generally the one(s) with:
   - Low defectivity (measured with defect inspection)
   - Low variability (measured with metrology)

Available KLA Workshops for Auto Fabs, Tier 1s, and OEMs

- Latent Reliability Defects
- Fab-wide Baseline Defect Reduction Strategies
- Inspection and Metrology Strategy Re-Optimization with DR Shrink
- Excursion Monitoring Optimization
- Die Level Screening Methodologies (inline)
- Micro-Excursions and Yield Variation
- Improving Cycle Time
- Sampling Optimization (% lots, wafers/lot, area/wafer, sites/wafer, SEM review)
- Virtual Metrology and Fault Detection
- Precision, Accuracy, and Misclassification Risk
- Using Metrology to Expand the Process Window
- Others upon request…

For more information, please contact Kara.Sherman@kla.com

Thank You